A New Design for 7:2 Compressors

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Abstract

High order compressors play a specific role in realizing high speed multipliers. By increasing the demand for fast multiplication process, high order compressors have attracted many researchers to this field. In this paper a new implementation for 7:2 compressors, based on the conventional architecture, is proposed. According to the results, the design presented achieves a remarkable improvement in terms of speed (especially in low voltages) and power consumption over the best counterpart. This accomplishment is the direct result of shortening the critical delay path in the proposed circuit design. As the simulation results demonstrate, the structure presented here has improved the power consumption from minimum 0.07 % (at supply voltage = 3.5 volt) through maximum 11% (at 1.2 volt), and the speed of the circuit from minimum 19 % (at 3.5 volt) through maximum 23 % (at 1.2 volt). HSPICE is the circuit simulator used, and the technology being used for simulations is 0.25μm technology.

1. Introduction

The speed of multipliers is a critical issue in determining the performance of microprocessors. Microprocessors use multipliers within their arithmetic logic units, and digital signal processing systems require multipliers to implement DSP algorithms such as convolution and filtering. The demand for high-speed multipliers is continuously increasing. The fast multiplication process consists of 3 steps: partial product generation, partial product reduction and final carry-propagating addition. Various recoding schemes are used to reduce the number of partial products. Compressors have been widely used for reduction process which usually contributes the most to the delay, power and area of the multiplier. To achieve a better performance, the use of higher order compressors instead of conventional compressors, e.g. 3:2 compressors, have been considered. The reduction process finally results in a 2-row matrix, and then a high speed adder is used to get the final result from the two rows [4]-[13].

In this paper a new implementation based on the conventional 7:2 architecture is proposed to be used for fast multiplication or multiple addition applications. The proposed 7:2 compressor and the most efficient contender have been simulated using HSPICE 0.25um technology. The results show a drastic improvement, as will be discussed later.

Previously, 3:2 compressors were used to reduce the partial product matrix; each reduces the number of inputs by a factor of 3:2. Thereafter, for the purpose that the compression rate might be increased, other higher order compressors have been developed. This attempt has yielded a faster partial product compression than the use of 3:2 counters.

2. Previous works

Taking a brief look at 7:3 compressors, which have stabilized a known position in related designs and provided the basis for our work, indicates that a typical realization uses four 3:2 counters, involving a critical path delay of 5 XORs and the compression ratio of 7/3 (which is much more than 3:2 counters).

Before the new implementation method for unconventional advanced compressors was introduced by [1], 7:2 compressors were realized using common methods, which involved a critical path delay of 7 XORs. Figure 1 shows this realization. The architecture uses 5 full adders combining 11 equally weighted bits to produce 6 bits: one (the sum) with weight of n, one (the carry) with weight n+1, and four additional carry out bits to the one greater significant cell with weight n+1 [1], [2].

In [1], a new implementation based on the idea of sending/receiving carry signals to/from more than one lower/greater significant cell was suggested, which not only reduced the number of stages required to eliminate carry propagation, but also halved the interconnections

resulting in less silicon area. Figure 2 depicts how a 7:3 compressor can be transformed to a 7:2 compressor by this method.

As might be evident, a 3:2 counter has been dragged from the final addition stage to the stage above, merging two stages at the expense of increasing 4 carry inputs and outputs connections. Although, the advantage of producing two outputs simultaneously is worth this drawback. This implementation has also 7 XORs delay.

Figure 3 illustrates a more detailed block diagram of the mentioned 7:2 compressor, the equations of which are written below:

$$
\begin{aligned}
c_1 &= (x_2 \oplus x_3).x_4 + (x_2 \overline{\oplus} x_3).x_2 \\
c_2 &= (x_5 \oplus x_6).x_7 + (x_5 \overline{\oplus} x_6).x_5 \\
c_4 &= (x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus x_6 \oplus x_7).x_1 \\
&\quad + (x_2 \overline{\oplus} x_3 \overline{\oplus} x_4 \overline{\oplus} x_5 \overline{\oplus} x_6 \overline{\oplus} x_7).s_3 \\
&= (x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus x_6 \oplus x_7).x_1 \\
&\quad + (x_2 \overline{\oplus} x_3 \overline{\oplus} x_4 \overline{\oplus} x_5 \overline{\oplus} x_6 \overline{\oplus} x_7) \\
&\qquad .(x_2 \oplus x_3 \oplus x_4)
\end{aligned}
\tag{1}
$$

3. Design of a new 7:2 compressor

By using the conventional 7:2 architecture as basis and changing its internal equations as follows, our proposed implementation (Figure 4) could achieve a better performance. In our novelty the critical path delay equals 6 XORs, which means the overall delay is reduced by one XOR as compared to the conventional counterpart. Applying the following changes to the above equations reduces the relation between the sum and carry generating trees and thus causes.

$$
\begin{aligned}
c_1 &= (x_3 + x_4) \cdot x_2 + x_3 \cdot x_4 \\
c_2 &= (x_6 + x_7) \cdot x_5 + x_6 \cdot x_7 \\
c_4 &= (s_4 + x_1) \cdot s_3 + s_4 \cdot x_1 \\
&= \big((x_5 \oplus x_6 \oplus x_7) + x_1\big) \cdot (x_2 \oplus x_3 \oplus x_4) + (x_5 \oplus x_6 \oplus x_7) \cdot x_1
\end{aligned}
\tag{2}
$$

Once again, changing the internal equations yields a new realization with a 6 -XOR delay.

In [3] another structure has been disclosed, the critical path delay of which equals 7XORs (Figure 5). As seen, the counters in each gray polygon build a 4:2 compressor. Comparing the proposed implementation with this architecture (Figure 5) indicates that our implementation has less interconnections and XOR delays. It moreover reduces the number of stages required for eliminating carry propagation delay from 3 stages to 2.

4. Choosing basic circuits

As clearly illustrated, all implementations have XORs and MUXs on their critical path.

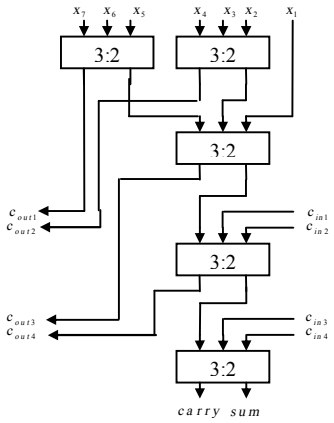

Figure 1. Common 7:2 compressor architecture (7Δ)

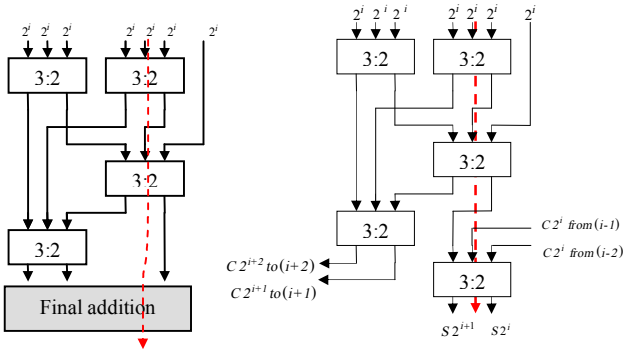

Figure 2. 7:2 compressor, conventional architecture (7Δ)

Hence, these blocks must be implemented efficiently. After investigating different implementations of XOR and MUX gates, the following choices have been made according to the simulation results for computing power-delay product, drivability and silicon area (Figure 6, 7) [14]-[19].

5. Simulation results

Hereafter, the proposed design and the best counterpart (the conventional structure) are simulated and compared. Our simulation structure is shown in Figure 8. According to the simulation setup, 3 maximum delay probable paths exist with respect to the input patterns, 2 of them are

shown in the figure, and the third one is the path from the inputs to the outputs. As previously mentioned, in the new architecture the number of stages required to eliminate carry propagation delay is two. However, a three cascading 7:2 compressor model is used due to sending a carry output to two greater consequent cells.

The following performance criteria are considered in evaluation of simulated 7:2 compressors, which are the average power consumption, critical delay path and power-delay product (Figure 9). Table 1 and 2 show the results. Simulation curves also indicate the superiority of the proposed realization to its rival.

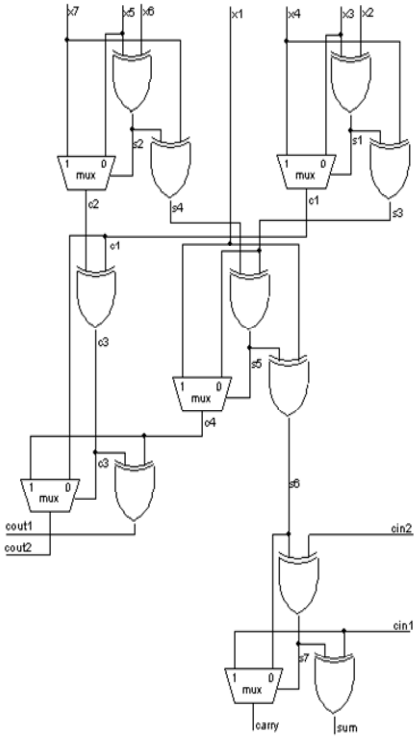

Figure 3. 7:2 compressor, conventional gate level architecture (7Δ)

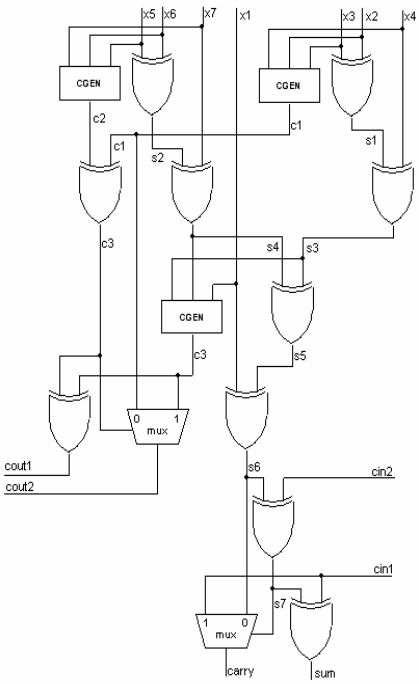

Figure 4. Proposed 7:2 compressor (6Δ)

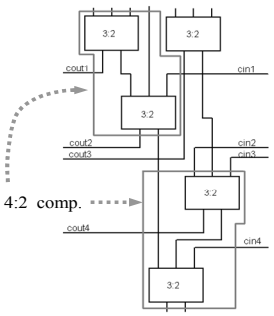

Figure 5. 7:2 compressor, [3] architecture (7Δ)

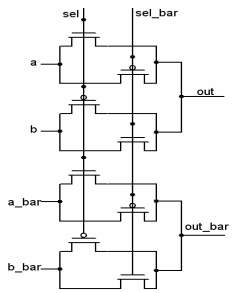

Figure 6. Selected multiplexer (DPL)

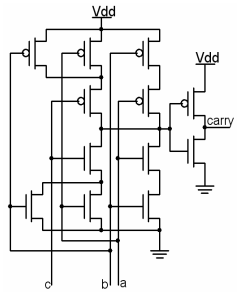

Figure 7. Selected carry generator

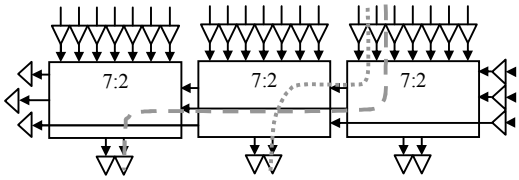

Figure 8. Simulation setup

Table 1. Number of delay stages

	conventional architecture	Proposed architecture
No. of Stages	7 Δ	6 Δ

Table 2. Evaluation of the proposed 7:2 compressor

	Min. (3.5v)	Max. (1.2v)
Improvement in power consumption	0.07 %	11 %
Improvement in speed	19 %	23 %

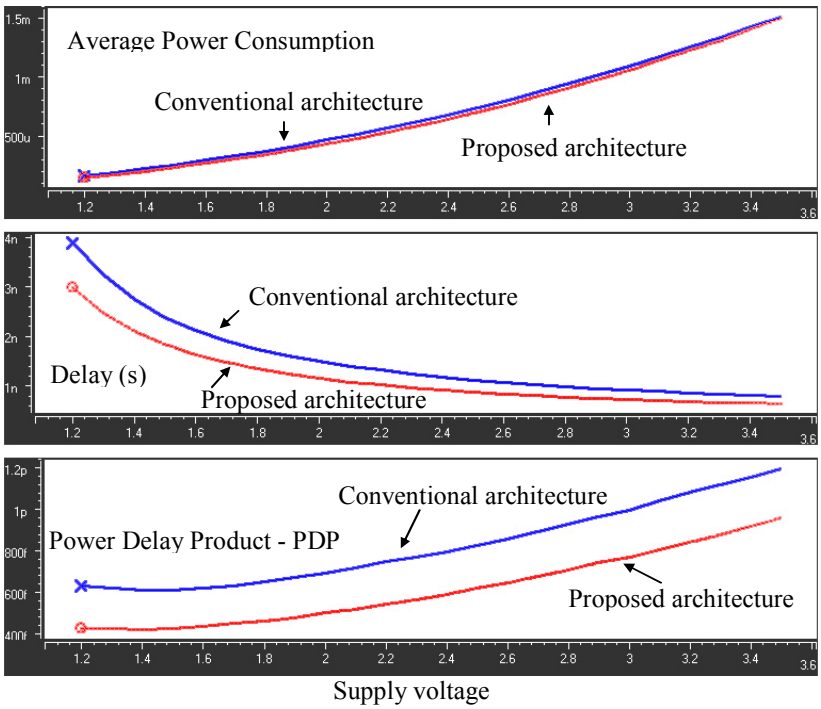

Figure 9. Power consumption, delay and power delay product curves

6. Conclusion

In this paper a novel circuit realization for 7:2compressor has been proposed and compared to the optimal counterpart. According to the results, a remarkable improvement in terms of power consumption (especially in low voltages) and speed is achieved. As the simulation results demonstrate, the structure presented here has improved the power consumption from minimum 0.07 % (at supply voltage = 3.5 volt) through maximum 11 % (at 1.2 volt), and the speed of the circuit from minimum 19 % (at 3.5 volt) through maximum 23 % (at 1.2 volt). The simulations have been performed by HSPICE simulator, in 25µm technology.

7. Reference

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