

Design and Analysis of Low Power Multipliers and 4:2 Compressor Using Adiabatic Logic

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Abstract- For high speed applications, a huge number of adders or compressors are to be used in multiplications to perform the partial product addition. In this paper a new approach of reducing power for a given system is developed that is adiabatic logic. The Array multiplier, Vedic 4x4 multiplier and 8x8 multiplier are designed using energy recovery logic in the inverter. The number of adders is reduced by introducing special kind of adders that are capable to add five/six/seven bits per decade. These adders are called compressors. A 4:2 compressor is developed using adiabatic logic for multiplier in order to reduce the power with facilitation of low power logic technique. The Vedic multiplier is designed using the compressor and the power results are obtained using TANNER EDA 12.0 tool. This paper presents a novel scheme for analysis of low power multipliers using adiabatic logic in inverter and in the compressor.

Keywords- Adiabatic logic, Compressor, Multipliers.

I. INTRODUCTION

Recently, power consumption has been a fundamental constraint in both high-performance and portable, energy-limited systems. In CMOS circuits, power dissipation primarily occurs during device switching. A sudden flow of current through channel resistive elements results in half of the supplied energy being dissipated at each transition. In CMOS technology, as $E_{diss} = \frac{1}{2} CL V_{dd}^2$, circuit designers are focusing on how to reduce V_{dd} and C_L . However, power dissipation can also be reduced by reducing the current flow into the transistors. In conventional CMOS circuit charging and discharging are done by PMOS and NMOS circuit. In this discharging energy is wasted through NMOS. Its waste in every charge and discharge cycle. In order to reuse the wasted energy we are going for adiabatic logic [2]. The 1:2 mm standard CMOS technology is purposely being performed because of this paper's focus, which is to reduce the dynamic power consumption. The first adiabatic logic family that we are going to discuss is split-level pulse adiabatic logic. It comprises a conventional CMOS gate with two complimentary split-level pulse voltages.

The peak voltage of each block supplies $v_{dd}/2$ to the gates. In this logic family, the dissipation occurs solely from a finite rate of change of driving voltage and can be decreased to any desired level. It has basically two drawbacks: - it is not suitable for pipelining and it is difficult to design [8].

A variety of adiabatic logic architecture has been proposed for low power VLSI design. Most of them use diodes for precharge, which cause unavoidable energy loss due to the voltage drop across the diodes; however they have potential problem of floating nodes and faulty logic [3]. This paper states that operation is based on diode free i.e. transistor connected as a diode of reduced voltage drop [5]. The architecture of the 3-2, 4-2 and 5-2 compressor are analysed using CMOS and CMOS+ implementation of 3T XOR and the MUX blocks reduces the power consumption and delay [9].

The remainder of the paper is organized as follows. Section II provides a brief description of the structure and operation of 2N-2P inverter and 4x4 bit array multiplier. Section III introduce a 4:2 compressor using adiabatic logic to optimized the Vedic 4x4 multiplier and 8x8 Vedic multiplier. Section IV presents the simulation and measurement results of the above mentioned low power multipliers. The last section concludes the paper.

II. INVERTER (2N-2P)

The figure 1 shows a circuit diagram of the 2N-2P inverter as compared to its CMOS equivalent. The 2N-2P inverter implementation uses a two-phase clocking split-level sinusoidal power supply, wherein V_f and V_r replace V_{dd} and ground, respectively. The voltage level of V_f exceeds that of V_r by a factor of $V_{dd}=2$ as shown by Equations (1) and (2).

$$V_{\theta} = \frac{V_{dd}}{4} \sin[(\omega t + \theta)] + \frac{3}{4} V_{dd} \quad (1)$$

$$V_{\theta} = -\frac{V_{dd}}{4} \sin[(\omega t + \theta)] + \frac{1}{4} V_{dd} \quad (2)$$

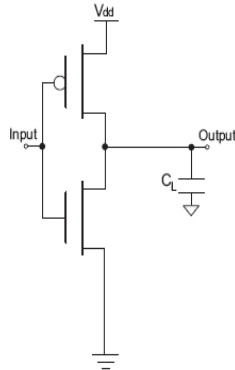


Figure 1. (a) CMOS Inverter

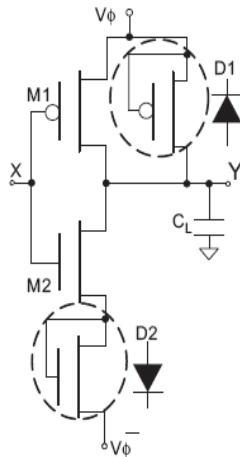


Figure 1. (b) Inverter 2N-2P

Where the voltages between current-carrying electrodes must be zero when the transistor switches to the on state. Consequently, power consumption is minimized. In figure 1(b) the MOSFET diodes are used to recycle the charge from the output node and to improve the discharge speed of the internal signal nodes. A method for reducing energy dissipation in inverter involves the design of a charging path without diodes. In energy-recovery circuits, according to the law of energy conservation, dissipated energy is equal to the total energy injected into the circuit, E_i , and the energy received back from the circuit capacitance, E_r .

$$P = 1/T \int_0^T (\sum_{i=1}^n (V_{pi} I_{pi})) dt \quad (3)$$

The circuit operation is divided into two phases, namely, evaluation and hold.

(a) *Evaluation phase:*

(a) When Y is LOW and the PMOS tree is turned ON, CL is charged through the PMOS transistor. Hence, Y is in the HIGH state.

(b) When node Y is HI and NMOS is ON, discharging via M1 and M4 occurs. Hence, Y is in the LOW state.

(b) *Hold phase:*

At the point when the preliminary state of Y is HIGH and the PMOS is ON, no transition occurs.

(A) *3T XOR*

The design of the full adder is based on the design of the XOR gate. The proposed design of full adder uses three transistor XOR gates. The design of a three transistor XOR gate is shown in figure 2.

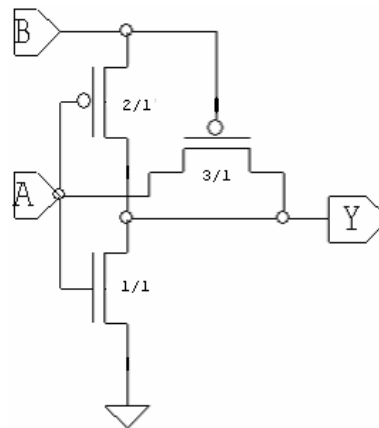


Figure 2. 3T XOR GATE

When the input B is at logic high, the inverter on the left functions like a normal CMOS inverter. Therefore the output Y is the complement of input A. When the input B is at logic low, the CMOS inverter output is at high impedance. This design of proposed full adder is based on 3T XOR. It acquires least silicon area. The heart of the design is based on a modified version of a 2N-2P inverter and a PMOS pass transistor.

(B) *4*4 bit array multiplier*

The 4*4-bit array multiplier consists of 16ANDs, six full adder logic circuits, and four half adder logic circuits are shown in the figure 3. For fabrication, D-flip flops are also used to capture all of the 8-bit signals when the clock is in the HI state.

The simulation results obtained using 1:2-mm CMOS technology for the 4*4 bit array multiplier and conventional CMOS multipliers were compared to the measurement results. The power dissipation results obtained from simulations and measurements. The transition frequency varied from 50 kHz to 5MHz.

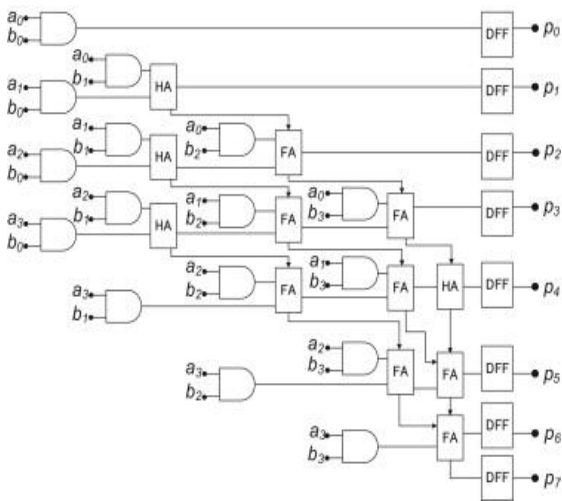


Figure 3. 4X4 Bit Array Multiplier

III VEDIC 4* 4 BIT MULTIPLIER

The proposed Vedic multiplier is based on the “Urdhva Tiryakbhyam” sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. It literally means “Vertically and crosswise”.

It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The figure (4) Multiplier is based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

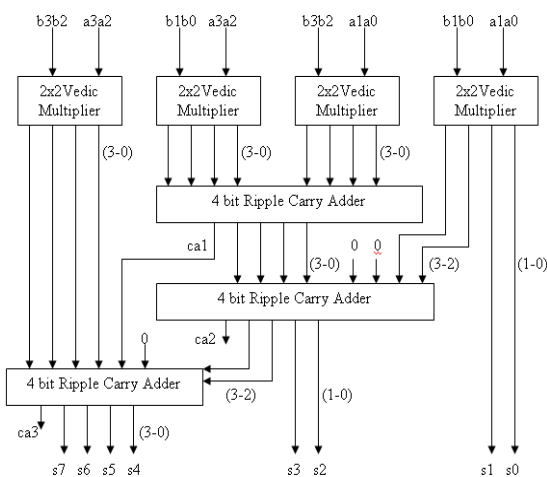
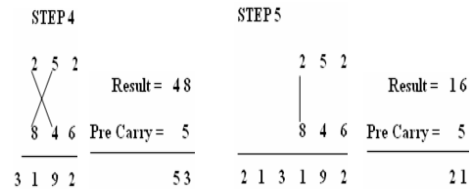
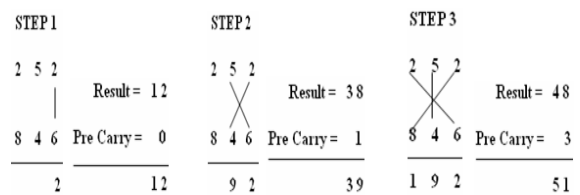


Figure 4. Vedic 4*4 Multiplier.

To illustrate this scheme, let us consider the multiplication of two decimal numbers $252 * 846$ by Urdhva Tiryakbhyam method. The digits on the both sides of the line (say, 2 and 6) are multiplied ($6 \times 2 = 12$) and added with the carry from the previous step (initially, carry=0). This generates one of the bits of the result (i.e. 2) and a carry (i.e.1). This carry (1) is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, Least Significant Bit (LSB) acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.



$252 \times 846 = 213192$

(A) 4-2 COMPRESSORS

The 4-2 compressor is another widely used building block for high precision and high speed multipliers. The block diagram of a 4-2 compressor is shown in the figure (5), which has four inputs and three outputs.

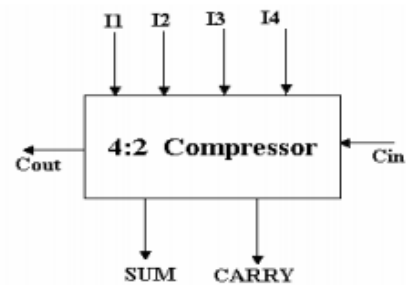


Figure 5. 4:2 COMPRESSOR

In 4-2 compressor block, four of the inputs are the primary inputs X_0, X_1, X_2 and X_3 and the output sum has some weight. C_{in} is the output carry of preceding module and C_{out} , the carry output of this stage is fed to the next compressor. The output carry is weighted one binary bit order higher.

The compressor is governed by following basic equation:

$$X1+X2+X3+X4+Cin= Sum+2*(Carry+ Cout) \quad (4)$$

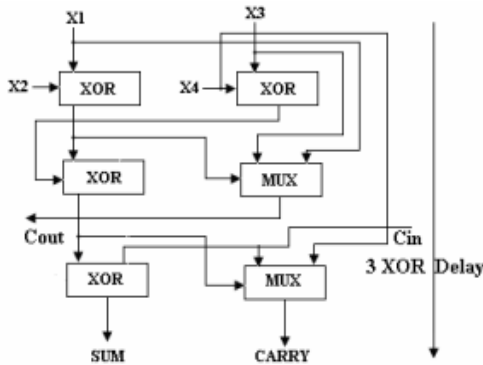


Figure 6. 4:2 Compressor using Full adder.

The conventional architecture of a 4-2 compressor is composed of two serially connected full adders are shown in the figure 6. To reduce the critical path delay, optimization is done at gate level.

The 4:2 compressor is used in Vedic multiplier instead of 5 inputs full adder. Whereas this 5inputs full adder is compressed by 4:2 compressor. The result of Vedic multiplier using compressor is compared with 4x4 Vedic multiplier.

(B) VEDIC 8*8 MULTIPLIER

An 8-bit VEDIC multiplier is made using four, 4 bit Vedic multipliers and three, 16 bit adders. The design is then simulated in Tanner tool. The smallest sub-circuit instance being used here is of a full adder. The systematic design flow then includes a 4-bit Vedic multiplier and finally the 8-bit Vedic multiplier. The 8x8 bit Vedic multiplier module as shown in the block diagram in Figure 7.

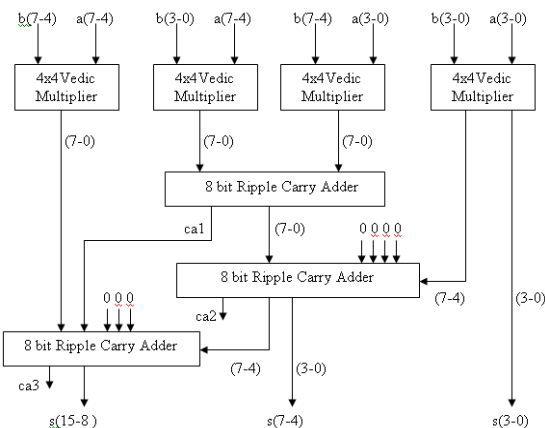


Figure 7. Vedic 8*8 Multiplier.

Let's analyse 8x8 multiplications, say A= A7 A6 A5 A4 A3 A2 A1 A0 and B= B7 B6 B5B4 B3 B2 B1B0. The output line for the multiplication result will be of 16 bits as – S15, S14, S13, S12, S11, S10, S9, S8, S7, S6, S5, S4, S3, S2, S1 & S0. Let's divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as:

$$P = A \times B = (AH-AL) \times (BH-BL)$$

$$=AH \times BH+(AH \times BL + AL \times BH)+AL \times BL \quad (5)$$

Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total three 8 bit Ripple-Carry Adders are required. The 8x8 bit Vedic multiplier is simulated using Tanner EDA (Electronic Design Automation) tool. The power and energy results are analysed. It is optimized for low power as well as high speed implementation advantageous when applied to low-power digital devices operated at low frequencies.

IV. SIMULATION RESULTS

For the overall analyses of the multipliers using adiabatic logic, we carried out the following power results value and the simulation is carried out using TANNER EDA 12.0 Tool. The average power consumed results are exposed in Table 1-2. Thus, this technique 57% of energy is saved when compared with conventional CMOS.

Table 1. Average power comparison of logic and multiplier

LOGIC FAMILIES	DESIGN NAME	AVERAGE POWER CONSUMED (mW)
CMOS	Inverter	1.245
Adiabatic (2N-2P)	Inverter	0.0644
2N-2P	Array multiplier	7.6324 e-002

AVERAGE POWER CONSUMED (mW)

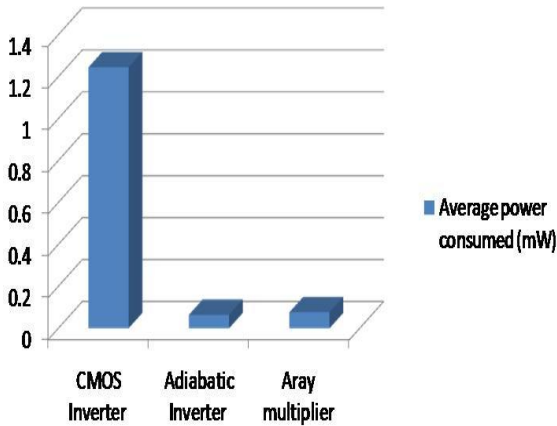


Figure 8. Power plot for Table 1.

Table 2.
Average power comparison of multipliers.

LOGIC FAMILIES	DESIGN NAME	AVERAGE POWER CONSUMED (W)
CMOS	4x4Vedic multiplier	2.0288e-002
Adiabatic (2N-2P)	Compressor	1.3205e-10
2N-2P	4x4Vedic multiplier	1.29063e-002
2N-2P	8X8Vedic multiplier	6.4235e-002

AVERAGE POWER CONSUMED (W)

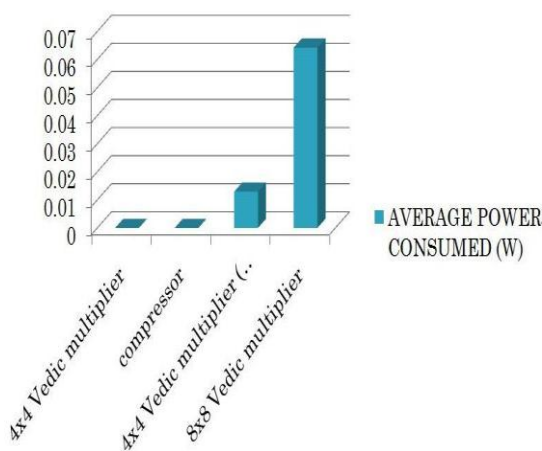


Figure 9. Power plot for Table 2.

V. CONCLUSION

This paper primarily was focused on the design of low power CMOS cells structures, and proposed energy efficient adiabatic logic technique in inverter and compressor. The multipliers circuit are designed and compared with conventional CMOS multiplier. The power and energy results are analysed. Thus adiabatic logic consumes less power and energy loss when compared with conventional CMOS.

It was found that the proposed adiabatic logic style is advantageous when applied to low-power digital devices operated at low frequencies, such as radio- frequency identification (RFID) tags, smart cards, and sensors.

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