Chapter 9

Overview and design of solid-state transformers

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9.1 Solid-state transformer: concept

The concept of electronic transformer was first introduced by [1] in the end of 1960s, where the main concept would be to adjust the output voltage by using the power electronics, while contributing to size and volume reduction. The apparatus in question isolated the primary and secondary side in frequency higher than the grid frequency and for that reason the size, weight and volume could be considerably reduced. At that time, there was no real applicability for such apparatus, mainly because of the performance limitation of the available semiconductors on the market.

However, with the advancement of the power electronics and semiconductors technology, new faster devices with lower switching energy were developed, enabling faster switching frequency operation. As a result, the volume and size of the power converters were considerably reduced, bringing advantages for those applications in which the power density is very important. At the same time, the classic solution used in traction for the electric locomotive was very heavy, bulky and inefficient, because of the low frequency transformer (LFT) employed [2] associated to the power electronics converters required for providing the suitable dc voltage to the variable speed drive on the locomotive. In this sense, the power electronics transformer or solid-state transformer (SST), as usually called, could provide the suitable controlled and isolated dc voltage in a unique solution, offering either volume and weight reduction (around 20%–50%) and efficiency improvement (from 93% to 96%) [2,3]. Thus, the SST became a reality in traction applications.

Figure 9.1 illustrates the conventional solution (state of the art) used on the locomotives, as well as the modern solution based on SST. The benefits offered by the SST in traction application are mainly on volume and weight reduction. Thus, the advantages of the system are only related to its hardware. The SST has been frequently conceptualized as presented below.

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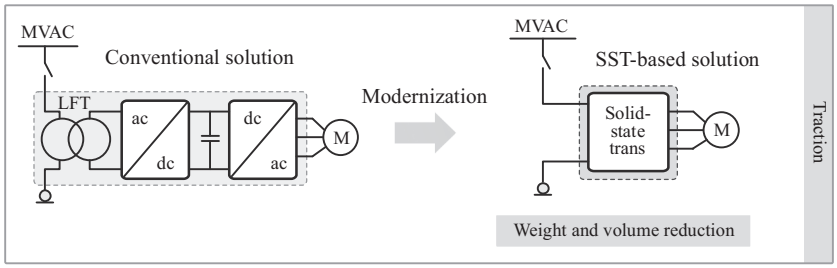

Figure 9.1 Solid-state transformer in traction application. MVAC, medium voltage ac; LFT, low frequency transformer

Solid-state transformer (SST):
Power electronics-based system with galvanic isolation in medium or high frequency between the input and output having waveform conditioning capability. It is normally employed to replace the traditional transformer, offering advantages in volume and weight reduction. Thus, the advantages offered by the SST are related to its hardware stage.

9.2 SST in electric distribution grid application

Apart from the advantages achieved in terms of hardware, the power electronics involved in the SST enables the implementation of an advanced control strategy with multiple control loops (e.g., power, voltage and current). This extra ability enlarges the SST application to other fields, such as electric distribution system, in which power and voltage control is the central requirement. Thus, the SST is very suitable for electric distribution system application, because it can perform as an LFT (replacing it), while providing ancillary services to the grid through its high-advanced control platform, improving the overall power quality of the distribution grid. Therefore, this technology has received a lot of attention in the research community (even academia and industry), and it was cited as one of the most emerging technologies by Massachusetts Institute of Technology Review in 2010 [4–6].

The new functionalities in the form of ancillary services to the electric grid are discussed in [3,7]. Among them, the reverse power flow condition, storage integration, management of hybrid grids (dc and ac) and power quality improvement are highlighted. Then, in this application, the SST is not only supposed to replace the conventional LFT, connecting the medium-voltage (MV) grid to the low-voltage (LV) grid, but also to offer dc connectivity and services to both LV and MV grids, as highlighted in Figure 9.2. In this case, weight and volume advantages have a limited impact, while the efficiency, reliability and functionalities are the primordial requirements. The aforementioned functionalities, enabled by the advanced software communication and control system, make the SST a smart

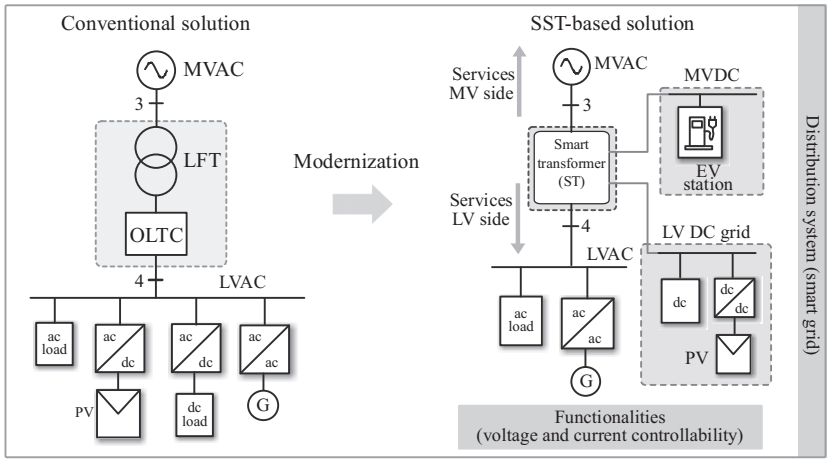

Figure 9.2 Solid-state transformer in electric distribution grid application, including the connection to dc grids

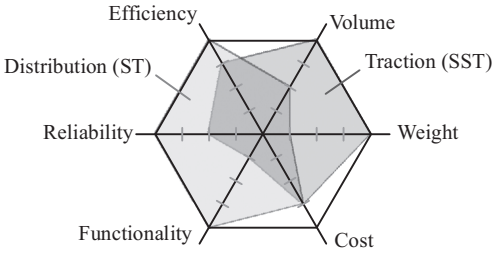

Figure 9.3 Requirements and performance of the SST and ST for traction and distribution grid applications

device, leading to the concept of smart transformer (ST). Then the ST can be conceptualized as described below.

Smart transformer (ST):
Power electronics based system with a galvanic isolation in medium or high frequency between the input and output with extra control functionalities, obtained through advanced communication and control system. In addition to the hardware advantage, its enhanced control makes the ST a powerful technology able to provide ancillary services to the distribution grid, solving most of the problems posed by the grid modernization. This system is a remarkable technology able to fulfill most of the requirements for the implementation of a smart grid, either ac or dc.

Figure 9.3 shows the main requirements and performance of the SST for both described applications. While the volume and weight reduction are the most

important requirement for traction application, the functionalities, reliability and efficiency play the most important roles in the electric distribution grid application.

9.3 ST architecture classification

The need to guarantee high efficiency and high reliability, offering new functionalities, has a direct impact on the ST architecture selection. To assist a proper structure selection, Figure 9.4 provides an overview of the possible architectures.

9.3.1 Power conversion stages

The most discussed classification is regarded the number of power conversion stages, that can be single-stage, two-stages or three-stages. The single-stage is normally implemented by a direct isolated matrix converter, and it is characterized to have high power density, because of the absence of the dc-link capacitors. However, the LV and MV are not decoupled, limiting the control capability. The two-stage topology is usually based on the indirect matrix converter and an inverter. This structure might present up to one constant dc-link, improving the controllability in respect to the single-stage structure. However, the two-stage structure offers limited functionalities. The three-stage is implemented by an MV ac–dc converter, isolated dc–dc converter and an LV inverter. This topology has normally two dc-links, in which at least one is available for connectivity. The decoupling between MV and LV sides provides more degree of freedom for the

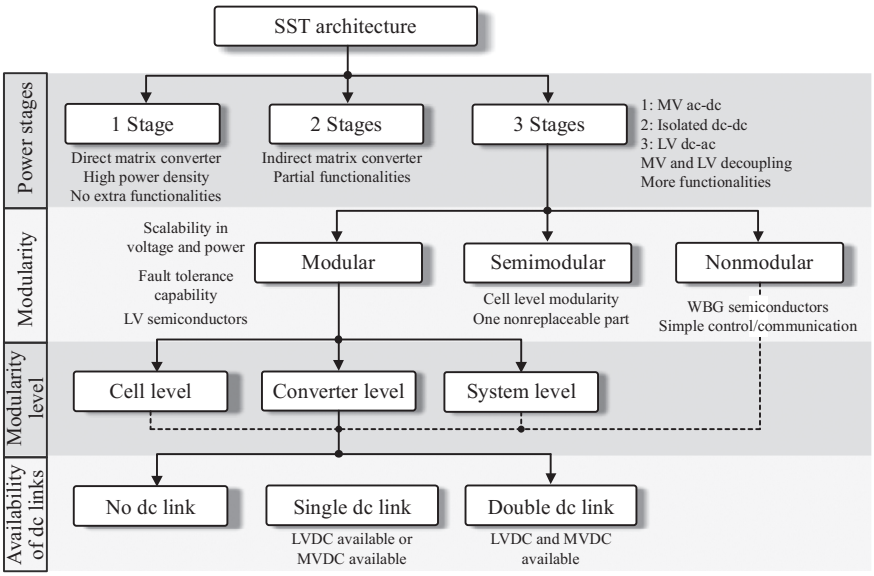

Figure 9.4 Classification of the ST architectures according to the number of power conversions, modularity and modularity level

system control, allowing the implementation of functionalities. Hence, this is the preferred architecture for the ST implementation.

9.3.2 Modularity

The next classification for the ST architecture concerns the degree of modularity. It can be classified as modular, nonmodular or semimodular. The nonmodular system is based on a single power converter, as exemplified in Figure 9.5(a), and usually takes the advantage of high voltage wide-bandgap (WBG) semiconductors [4,5,8]. Special devices with high blocking voltage capabilities, such as 10 kV Silicon Carbide (SiC) MOSFETs or 15 kV SiC IGBTs [9–11] are needed to handle the MV level in the power converter. Because these devices are not commercially available, but only for research purposes, no currently available products are using this technology. A standard approach to handle the MV in a nonmodular solution used in industrial applications is to employ semiconductor connected in series; however, this demands an additional control effort to balance the voltage over the semiconductors.

Conversely, the modular approach consists of several basic converters rated for LV or low current, which are used as building blocks for the entire system, as depicted in Figure 9.5(b). In this solution, the basic building block shares the voltage

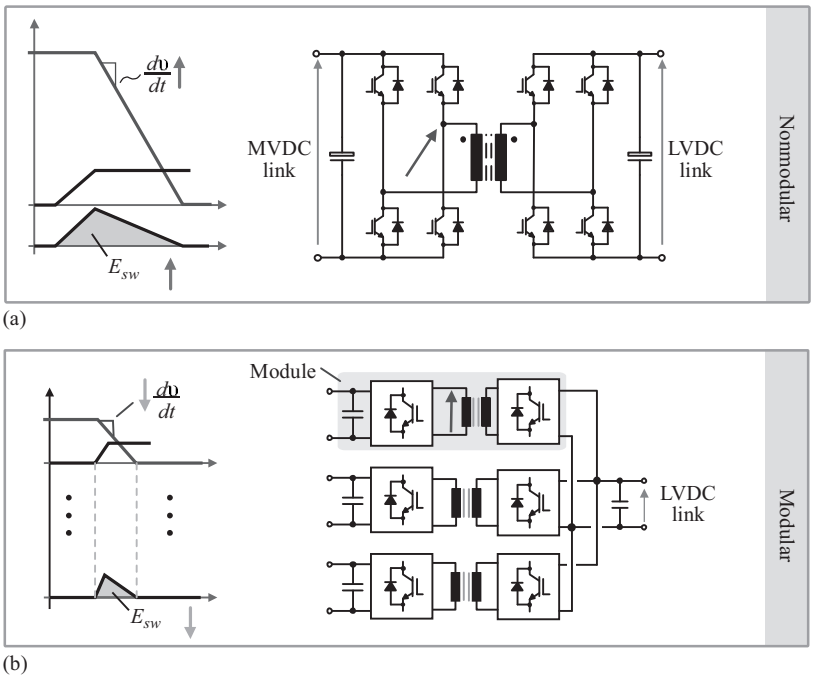

Figure 9.5 Possible implementation approaches of the ST architecture to handle the MV level involved in the power conversion: (a) nonmodular and (b) modular

on the MV side and the current in the LV among them, enabling the use of LV rated devices. In spite of the fact that more components are used compared to the nonmodular solution, the modular approach is more economically advantageous, as demonstrated in [12]. Additionally, modular architectures bring several advantages to the power and voltage scalability, maintenance and the implementation of fault-tolerant strategies. In comparison to the nonmodular, the modular architectures have reduced electromagnetic interference (EMI) emissions [due to the low dv/dt and di/dt, as illustrated in Figure 9.5(a) and (b)] and the possibility to use standard LV rated devices that perform well, benefiting both efficiency and cost.

Some features from the modular and nonmodular concepts can be combined to form the semimodular concept, as an alternative for both previous approaches. In this case, the architecture is implemented using basic modules sharing the power, similar to the modular approach, but a nonreplaceable component processing the total system power is part of the architecture. It can also be called as a partially modular approach, in which the modules on the primary side divide the power among them, while the high frequency transformer (HFT) and the secondary side bridge processes all the power.

9.3.3 Modularity level

The modular approach can be implemented in different level, as shown in Figure 9.6, and they are classified as cell level, converter level and system level.

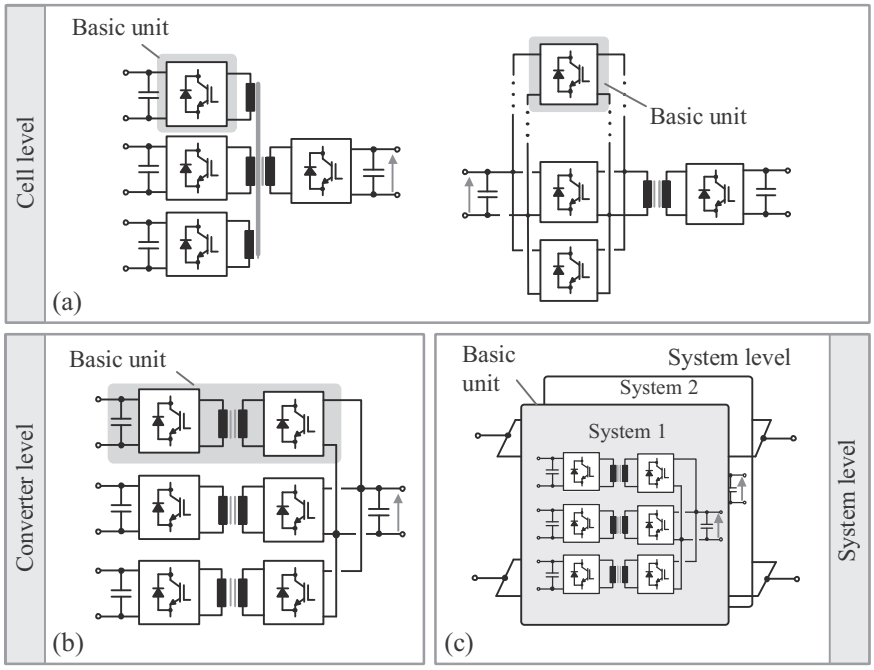

Figure 9.6 Modularization level: (a) cell level, (b) converter level and (c) system level

Cell level:
This is the most basic level, in which the basic unit is the cell used inside the converter, as exemplified in Figure 9.6(a). Another example of a cell-level modular system is the modular multilevel converter that is a single converter using several cells as basic units.

Converter level:
The next level is the converter level. In this case, the power converter is the basic unit, and they are combined in series and/or parallel to implement the entire system, as shown in Figure 9.6(b). This is the most employed modularization level and the input-series output-parallel connection is very popular. Interleaved converter is another example of the converter level modular system, in which several converters are connected in parallel.

System level:
Finally, the system level is presented in Figure 9.6(c). In this case, the full system is used as the basic unit. It is often used in application where fault-tolerance or scalability is highly desired.

All these levels can be freely combined, resulting in a modular system in multiple levels. In modular ST architectures, the converter level is the most common one, although the cell level can also be used.

9.3.4 dc Link voltage availability

The conceptualization of the ST is an important task during its conceivement, because it affects and constraints the further design phases. Besides the number of stages and the modularity level, another very important decision must be taken during the conceiving of the ST architecture: the availability of the dc link. Recently, the dc microgrid technology has been developed significantly, and many solutions for issues related to the grid stability and protection have been proposed in literature. This sort of grid is usually integrated to the ac grid through an LFT associated to a front-end rectifier for forming the required dc voltage. Alternatively, the dc microgrid can be connected directly to the dc link of the ST, so that its integration into the conventional ac grid happens through the ST. Hence, the ST technology enables efficiently the integration of the dc microgrid, and this feature play an important role during the conceptualization of the ST architecture.

The modular three-stage architecture has enough degree of freedom to provide one, two or even no connectivity to the dc links. It depends on the configuration of the power converters, as depicted in Figure 9.7 for a simplified single-phase structure. The availability of one dc link on the LV side (i.e., LVDC link) is the state-of-the-art and the most adopted option, enabling the dc microgrid connection [3–5].

The configurations without the LVDC link connectivity, as seen in Figure 9.7(a) and (c), have distributed dc links on the LV side, instead of having them

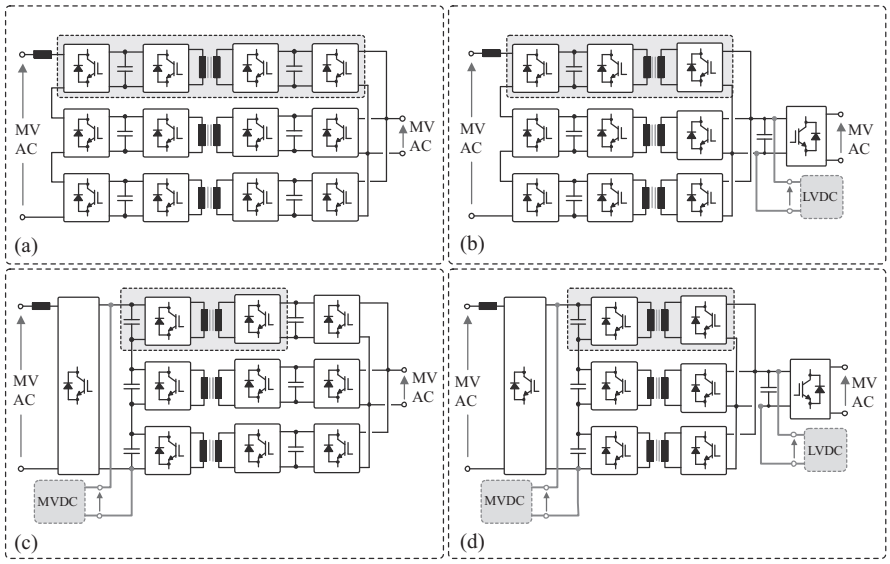

Figure 9.7 Different ST architecture configuration regarding the dc link connectivity for a simplified single-phase structure: (a) without dc link availability, (b) availability of the LVDC link, (c) availability of the MVDC link, (d) availability of both LVDC and MVDC links

connected. This strategy does not bring any advantages, and for this reason it has not being adopted [3]. On the other hand, the distributed dc links on the MV side provides advantages to the system, because the MV level involved in this side can be distributed among the modules. For this reason, this concept has been intensively used [3,4,12–16] and the most adopted structure is the one presented in Figure 9.7(b).

Recently, the availability of the MVDC link has been discussed by the research community, but there is no solution in this regard. The few amount of dc loads applicable for MV level compared to the LV one (which is already well established) makes the MVDC availability still controversial. Nevertheless, new dc loads in LV level are emerging (e.g., electric fast charging station), supporting research on the architectures with MVDC link. Consequently, the architecture with MVDC link as shown in Figure 9.7(c) and (d) is not well adopted yet, but it is a high potential structure and deserves attention.

In summary, the availability of the LVDC link is of paramount importance, and then two configurations with respect to the dc link connectivity are highlighted: the available LVDC link [Figure 9.7(b)] and the available LVDC and MVDC links [Figure 9.7(d)].

9.4 Solid-state transformer and smart transformer architectures overview

In the last two decades, many different SST and ST architectures have been proposed and discussed in literature for traction and distribution grid applications. The most relevant architectures used in both application are discussed.

In traction applications, the architectures are characterized to use commercialized HV Si-IGBT, two power processing stages, as well as modular approach. The efficiencies for each architecture for traction system are presented in Table 9.1. All of them provide higher efficiency and power density, when compared to the conventional solution using the LFT.

The three-stage architecture offers decoupling between the input and output, besides the availability of at least one dc link. Consequently, it is the preferable structure for grid applications, as seen in Table 9.1. To handle the MV level, two approaches are commonly used: modular with commercial LV devices and nonmodular with customized HV devices. Regardless the adopted concept, most of these architecture takes advantages of the high performance WBG SiC devices. They offer lower conduction and switching losses compared to the standard devices, and they are very promising in ST application.

Figure 9.8(a) shows the efficiency values available in the literature according to power of the system, as denoted in Table 9.1. For distribution system, very few ST demonstrators with solid results have been presented in the literature so far. The

Table 9.1 Comparison of the ST and SST architectures from different research groups/companies

Distribution application					
Name	**Project/group**	**Stages**	**Concept**	**DC link**	**References**
A	FREEDM	3	Modular	LV	[13]
B	FREEDM	3	Nonmodular	MV/LV	[11,17]
C	FREEDM	3	Nonmodular	MV/LV	[9,10]
D	ETH	3	Modular	LV	[18]
E	Uniflex	3	Modular	No	[19–21]
F	GE	2	Modular	No	[22]
Traction application					
Name	**Company**	**Stages**	**Concept**	**Efficiency (%)**	**References**
G	ABB	1	Modular	94.5	[23,24]
H	ABB	2	Modular	96.2	[14,25]
I	Alstom	2	Partially modular	94	[26,27]
J	Bombardier	2	Modular	96.2	[28]
K	Siemens	2	Partially modular	97	[29,30]

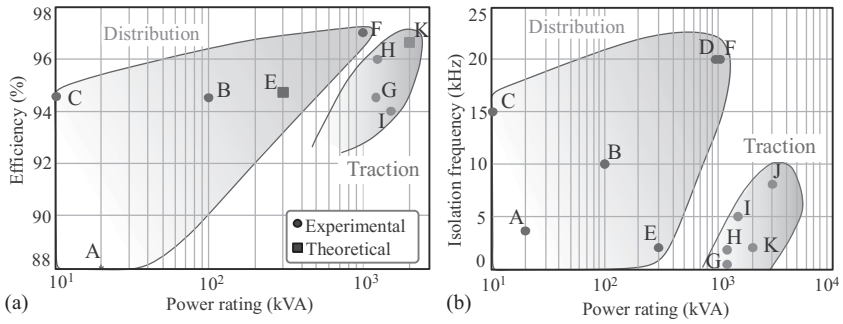

Figure 9.8 Performance comparison of the most relevant ST and SST architectures developed by industries and universities (see Table 9.1): (a) achieved efficiency compared to the power rating and (b) isolation frequency as a function of the power rating

available data shows that the efficiency achieved by this kind of system is around 94.5%–97%. For traction systems, the ST efficiency is in the range of 94.5%–96%, according to the available data provided experimentally (excluding the theoretical one). Although the ST architectures in the distribution use more power stages compared to those used in Traction, their performance is potentially higher, because the utilized WBG semiconductors that plays a very important role in this regards. Figure 9.8(b) shows the isolation frequency for each ST architecture shown in Table 9.1, according to the power level. In traction, the isolation frequency is normally below 10 kHz, whereas in distribution grid is mostly around 10–20 kHz. The limitation of switching frequency is ST for traction is explained by the fact of HV Si-IGBT are normally used to save cost. It results in more switching losses or switching frequency limitations.

9.5 dc–dc Stage: power converter topologies

The dc–dc stage is considered as the core element of the ST architecture, because it is responsible to connect the MV side to the LV side providing galvanic isolation in medium or high frequency among them. In consequence of its strict requirements discussed next, this stage is the most challenging for the implementation [3,16,18, 31,32]. The high voltage and current levels involved on the power conversion makes the dc–dc stage responsible for the majority of the system losses; hence, it deserves more attention during the ST design. Moreover, this stage controls the LVDC link, in which the dc microgrid is connected to. The requirements and a review of the possible solutions for the dc–dc stage is discussed next.

9.5.1 Requirements

The requirements for the dc–dc stage of the ST, independently of the adopted approach (modular or nonmodular), are summarized as follows:

- **High voltage capability in the MV side:** Handle voltage level of around 6–25 kV.
- **High current in the LV side:** Current level in the range of 100–2,000 A is expected [3].
- **High voltage isolation:** The MF/HF transformer employed has an isolation requirement defined by the own MVAC level, i.e., between 10 and 15 kV, regardless of the solution adopted for the dc–dc stage.
- **Decoupling degree between the MV dc side and the LV dc side:** Ability to provide total decoupling between the MVAC grid and the LVAC grid, so that the MV stage and LV stage converters can operate independently from each other. It means that the MV ac–dc stage can operate and provide the required ancillary services to the MV grid (e.g., provide reactive power), without disturbing or being disturbed by the LV dc–ac stage operation. The same remark is also valid for the LV dc–ac stage operation. To achieve such decoupling degree, both dc links (MV and LV) must be maintained constant with minimal oscillation voltage (i.e., 5% of the LVDC [3]), and the dc–dc converter should guarantee the voltage regulation.
- **Control of the power flow:** Ability to control the power flow between the LVDC link and MVDC link and manage the connection of loads of both sides [4,5,8].
- **Bidirectionality:** Many publications agree that the bidirectional power flow capability is required for the dc–dc stage [3–5,8,33]. On the other hand, this requirement is questionable, because the reverse power is an exceptional case in the distribution system. If economically viable, unidirectional solution could also be accepted. Despite that, bidirectionality is considered as a requirement in modern ST.
- **dc Breaker function:** Overload and short-circuit protection (working as a dc breaker) of the possible load/source/microgrid connected to the LVDC link) [3–5,8,33].
- **High efficiency:** The ST is not only intended to replace the LFT of the distribution system but also solve problems coming from the grid modernization [3]. However, high efficiency is expected for the ST, in order to compete with the LFT. The highest efficiencies obtained from an SST in traction applications are around 95%–97%, for two processing stages (i.e., ac–dc and dc–dc) [14]. Taking this fact into account, an expected efficiency of 96% is defined for the whole ST system, as shown in Figure 9.9(b). The MV stage can achieve an efficiency around 98.6%–99.3% [14,34], when multilevel converters are used, while the LV stage can offer an efficiency in the range of 98.8%–99.2% [35–37]. The dc–dc stage should provide an efficiency between 97.5% and 98.6%, so that the entire system achieves the desired efficiency, as shown in Figure 9.9. Thus, an efficiency goal above 97.5% can be defined.

9.5.2 Basic module topologies

From the dc–dc converter requirements, the high efficiency is the most severe one. The modular approach contributes a lot in terms of performance improvement of the ST, because this approach allows the use of lower voltage rated devices, which performs significantly better than those rated for higher voltage [3]. As described

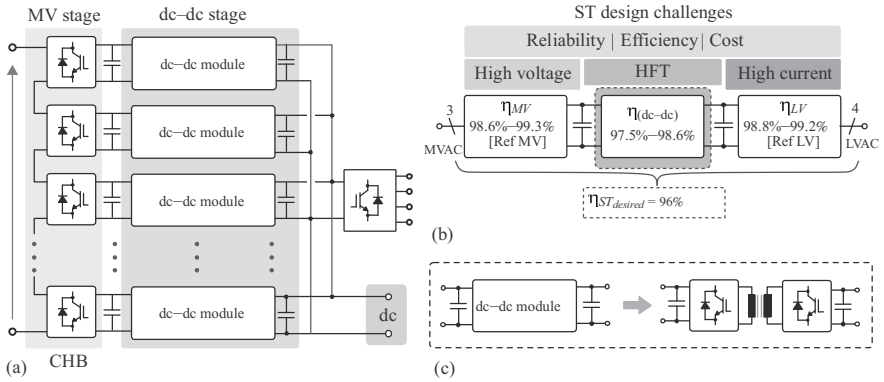

Figure 9.9 (a) Equivalent single phase modular ST architecture adopting the defined CHB, (b) expected efficiency for the whole system, as well as for each power conversion stage ([Ref MV] = [14,34], [Ref LV] = [35–37]), (c) implementation of the basic module of the modular dc–dc stage

Table 9.2 Specification range of the basic module of the dc–dc stage

Power level	5–100 kW
Input voltage	0.6–1.7 kV
Output voltage	600–800 V
Isolation frequency	1–40 kHz
Desired efficiency	>97.5%

before, this approach consists of several basic modules combined to build the entire architecture, as shown in Figure 9.9(a). The basic modules are isolated dc–dc converters, as depicted in Figure 9.9(c), and many topology options are available. The topology choice of the basic module plays an important role in the ST design, once the performance of the entire system depends on the efficiency of the individual module. The specification of the dc–dc basic module is usually in the range shown in Table 9.2. Considering this and the requirements described earlier, an overview of the most suitable topologies for the basic modules is presented as follows.

Among several options of the dc–dc converters, two families of converters are pointed out as the most promising: the SRCs and the active bridges converters.

9.6 Series resonant converter

The series resonant converter (SRC) is the most adopted converter in ST, considering the family of resonant converters, and its topology is presented in

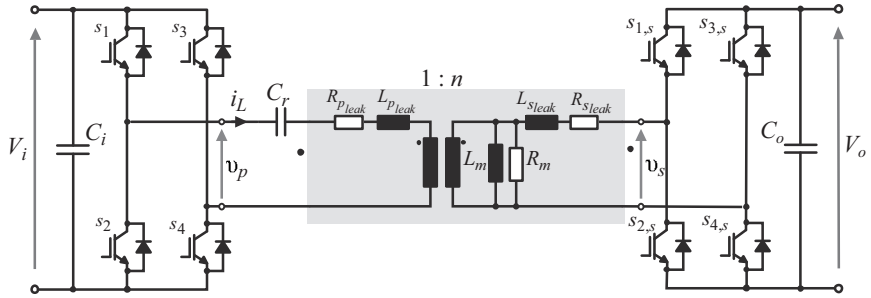

Figure 9.10 Topology of the series-resonant dc–dc converter

Table 9.3 Main parameters used on the analysis of the series resonant converter in Figure 9.10

Parameter	**Definition**
Angular switching frequency	$\omega_s = 2\pi f_s$
Angular resonant frequency	$\omega_o = 2\pi f_o$
Relative angular frequency	$\omega = \omega_s/\omega_s$
Resonant frequency	$f_o = 1/2\pi\sqrt{L_r C_r}$
Quality factor	$Q = 2\pi f_o L_r/R_a = 1/2\pi f_o C_r R_a$

Figure 9.10. The SRC converter is composed by a full-bridge converter on the primary and secondary sides, connected through a resonant tank circuit and a transformer. The tank circuit is composed of a resonant capacitor (C_r) connected in series to the resonant inductor (L_r). The SRC has different operation modes, according to the load and to the relationship between the switching frequency (f_s) and resonance frequency (f_o). The resonance frequency depends only on the pair L_r and C_r, and it is defined in Table 9.3. With respect to the load, the SRC can operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Regarding the switching frequency, it can operate below the resonant frequency, equal to the resonant frequency and above the resonant frequency [38].

Independent of the operation mode, the SRC converter can generally be analyzed according to [38–40]. In those works, the input–output voltage relation is derived, and it described in (9.1). Note that the variables presented in this equation are described in Table 9.3.

$$\frac{V_o}{V_i}(j\omega) = \frac{1}{1 + jQ((\omega_s/\omega_o) - (\omega_o/\omega_s))} \tag{9.1}$$

Figure 9.11(b) shows the normalized voltage gain (V_o/V_i) of the SRC as a function of the normalized operation frequency (f_o/f_s), according to the quality factor Q. According to this figure, the gain of the SRC varies with the frequency,

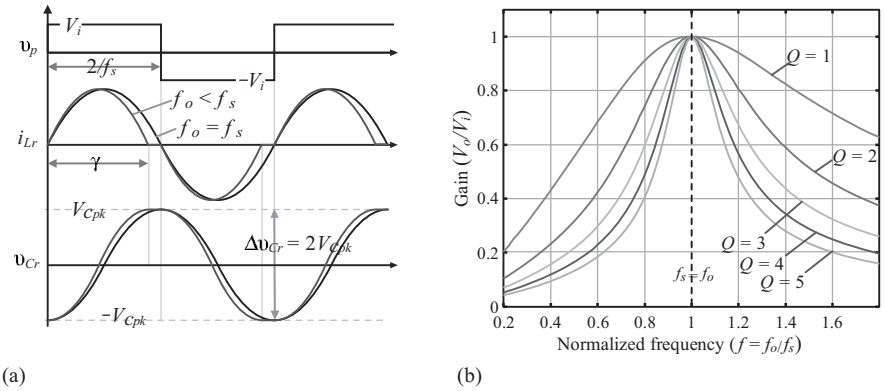

Figure 9.11 Series resonant converter: (a) main waveforms of the SRC and (b) normalized voltage gain (V_o/V_i) of the SRC as a function of the normalized operation frequency (f_o/f_s), according to the quality factor Q

and usually the switching frequency is used to control the output voltage of the SRC. However, this strategy implies a complex control system and poor utilization of the HFT, once it must be designed to operate for the minimum frequency. Thus, it is not suitable for ST applications, in which the power level is relatively high.

The most efficient operating point of the SRC is when it operates in the DCM with the switching frequency (f_s) equal or slightly below the resonance frequency (f_o), i.e., with unity gain. In this operation mode, the primary side switches achieve ZVS and the output diodes achieve zero-current-switching. Moreover, the converter has good transformer utilization and also low EMI emission due to the smooth current shape (low di/dt). In this operation point, the power flow is not directly controlled, and the power conversion between input and output is defined by (9.2), where n is the transformer turns ratio. On the other hand, it is not a disadvantage in ST application, once the system has enough degrees of freedom to control the input voltage by using the front-end rectifier (first stage).

$$V_o = n \cdot V_i \tag{9.2}$$

9.6.1 Current stress

To design the SRC converter, mapping the stresses on the semiconductors and transformers are required. They are normally calculated using waveforms illustrated in Figure 9.11(a) and using the concept of average and rms value. Using this approach, the mean value and rms value of the current in the semiconductors can be calculated using the equations shown in Table 9.4. Likewise, the current stresses on the transformer are calculated by the equations given in Table 9.5.

Table 9.4 Current stresses on the components S_{1b} (MV side) of the SRC [16]

Semiconductor	AVG	RMS
MV side	nP_o/V_o	$nP_o/8V_o\sqrt{2\pi/(f_s\sqrt{L_rC_r})}$
LV side	P_o/V_o	$P_o/8V_o\sqrt{2\pi/(f_s\sqrt{L_rC_r})}$

Table 9.5 Current stresses on the transformer of the SRC [16]

MV side	LV side
$nP_o/4V_o\sqrt{\pi/(f_s\sqrt{L_rC_r})}$	$P_o/4V_o\sqrt{\pi/(f_s\sqrt{L_rC_r})}$

9.6.2 Efficiency expectation

A high efficiency SRC is reported in [41] for high power and LV level applications (5 kW, 600 V). In that paper, SiC MOSFETs are used, presenting a peak efficiency of 97.6%, which is one of the highest efficiencies reported in the literature, considering the power/voltage level. Similarly, the SRC has been adopted in SST for traction applications in [14,25], where an efficiency of 98% was reported for a converter of 160 kW, employing special IGBTs devices.

Similarly, an optimum design of an SRC in ST application has been reported in [16]. In this paper, the authors proposed a design methodology to improve the efficiency and lifetime of the SRC, and the performance of the converter was evaluated considering different semiconductors. The converter provides an efficiency of 98.61%, when SiC-MOSFETs are used. Consequently, a very high efficiency can be expected for this kind of converter using WBG devices.

The main drawback of the SRC for ST application is the lack of controllability. The converter operates in open-loop, and it is not able to control the power flow. Consequently, the control of the LVDC link for dc microgrid connectivity must be shifted to other converter, when the SRC is used in the ST.

9.7 Dual active bridge (DAB) converter

The most popular converter of the active bridge family is the dual active bridge (DAB) and its topology is presented in Figure 9.12. The DAB converter is composed of two active bridges, connected through the inductance L_{DAB} and a transformer. Even though the DAB topology is similar to the SRC, its operation is totally different. Other topologies of the active bridge converter family, such as the three-phase DAB and the multiple-active-bridge (MAB), can also be adopted as a basic module of the ST. In fact, the MAB converter has been intensively

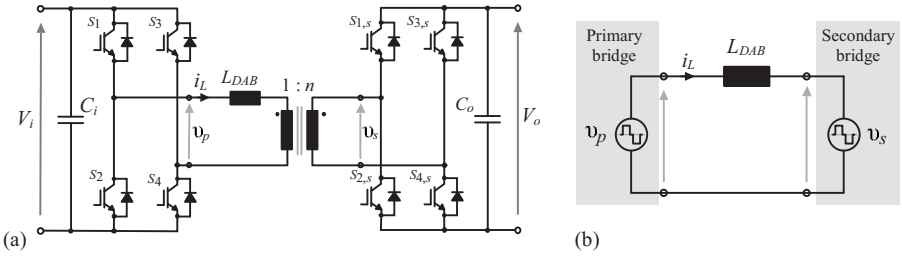

Figure 9.12 Topology of the dual active bridge (DAB) dc–dc converter (a) and its equivalent circuit (b)

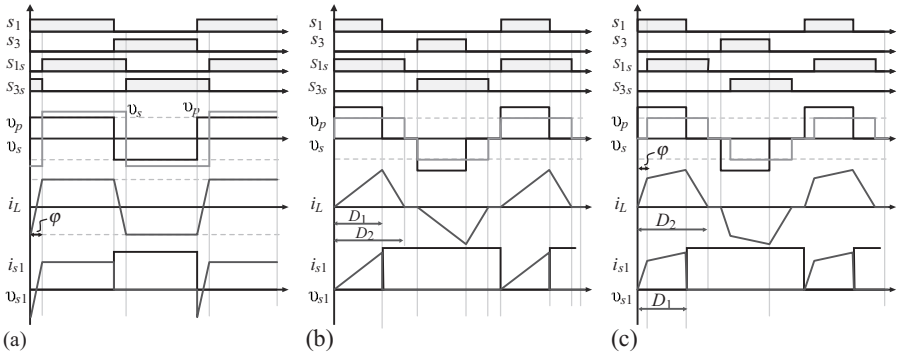

Figure 9.13 Main waveforms of the DAB converter considering different modulation strategies: (a) phase-shift modulation (PSM), (b) triangular current modulation (TCM), (c) trapezoidal modulation (TPM)

investigated for ST applications like in [42], and good results have been presented. However, the DAB converter is analyzed next for the sake of simplicity.

9.7.1 Modulation strategy

To modulate the DAB, many strategies have been presented [43–48], but the phase shift modulation (PSM) is the most adopted one. The main waveforms of the DAB using the PSM is depicted in Figure 9.13(a). In this scheme, rectangular voltages v_p and v_s with 50% duty-cycles and phase shift of φ are applied to the transformer with a constant switching frequency f_s. The power is controlled by the phase difference between the bridges. The PSM is characterized by ZVS turn-on of the semiconductors, low rms current, symmetrical share of the losses in all switches, high power transfer capability besides its simplicity. On the other hand, these advantages are obtained depending on the input–output voltage ratio and also the chosen operation point (nominal phase shift φ).

When the input voltage and/or output voltage of the converter deviate significantly from their nominal values (around 20%, according to [46,49]), the soft-switching operation is normally lost. In this condition, the PSM is not advantageous anymore [46]. To overcome this problem, alternative modulation strategies have been proposed, like the triangular current mode (TCM) and the trapezoidal modulation (TPM), as shown in Figure 9.13(b) and (c), respectively. The TCM imposes a triangular shape current on the transformer, while the TPM generates a trapezoidal current waveform on the transformer, as shown in (b) and (c), respectively. In contrary to the PSM, the TCM and TPM control the duty-cycle for transferring power between the input and output of the converter. These strategies can operate with soft-switching independently from the input and/or output voltage deviation, but with penalty on the peak value of the currents. To transfer the same amount of power, the DAB converter presents higher peak values of currents, when TCM and TPM are adopted in comparison with the PSM, because of the triangular or rectangular shape of the current. It means that the rms values on the semiconductors and transformers are also expected to be higher, implying on possible increase of the conduction losses.

In ST application, the input and output voltage are typically constant without large deviation of the nominal value. In this sense, the PSM is very advantageous, and therefore the DAB converter is analyzed next using this strategy.

9.7.2 *Analysis of the DAB using the PSM*

For the theoretical analysis of the DAB converter, the equivalent circuit shown Figure 9.12(b) can be used, where the active bridges are replaced by rectangular voltage sources v_p and v_s. The waveforms of v_p and v_s are shown in Figure 9.14. Analyzing the equivalent circuit, the inductor current is described by (9.3).

$$i_L(t) = i_L(t_0) + \frac{1}{L}\int_{t_0}^{t_0+T_s} v_L(t)dt = i_L(t_0) + \frac{1}{L}\int_{t_0}^{t_0+T_s} (v_p - nv_s)dt \tag{9.3}$$

The average power transferred can be defined by the following equation:

$$P = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} p(t)dt = \frac{2}{T_s}\int_{t_0}^{t_0+T_s/2} v_p(t)i_L(t)dt = \frac{2V_i}{T_s}\int_{t_0}^{t_0+T_s/2} i_L(t)dt \tag{9.4}$$

Considering the current waveforms shown in Figure 9.14, the inductor current can be described by (9.5). In this equation, the initial values are defined by (9.6) and (9.7), respectively.

$$i_L = \begin{cases} i_L(t_o) + \dfrac{v_p + nv_s}{L_{DAB}}t, & t_o < t < t_1 \\ i_L(t_1) + \dfrac{v_p + nv_s}{L_{DAB}}(t - t_1) & t_1 < t < t_0 + \dfrac{T_s}{2} \end{cases} \tag{9.5}$$

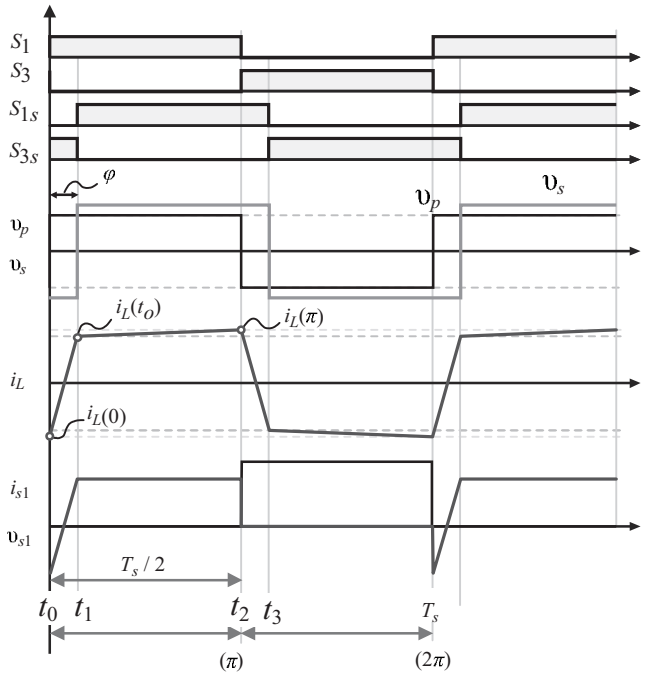

Figure 9.14 Voltage and current waveforms of the DAB converter operating with PSM

$$i_L(t_o) = -\frac{(V_i - nV_o)\pi - 2nV_o\varphi}{4\pi f_s L_{DAB}} \tag{9.6}$$

$$i_L(t_1) = \frac{(nV_o - V_i)\pi - 2V_i\varphi}{4\pi f_s L_{DAB}} \tag{9.7}$$

Note that $i_L(t_o) = -i_L(\pi)$ in steady-state condition. Replacing (9.5) in (9.4) and rearranging it, the equation of the power transference of the DAB is obtained, as shown in (9.8) [49]. The input–output voltage relation of the DAB can be defined as $d = nV_o/V_i$. The output power can be rewritten in terms of d, as shown in the following equation:

$$P = \frac{V_i V_o}{2\pi f_s L_{DAB} n}\varphi\left(1 - \frac{|\varphi|}{\pi}\right) = \frac{V_i^2}{2\pi f_s L_{DAB}} d\varphi\left(1 - \frac{|\varphi|}{\pi}\right) \tag{9.8}$$

The soft-switching is achieved when the devices are conducting at turn-off. This means that the condition $i_L(0) \leq 0$ and $i_L(\varphi) \geq 0$ must be satisfied. The requirement of $i_L(\varphi) \geq 0$ ensures the turn-off under ZVS of the switches s_1 and s_4 (see Figure 9.14), while $i_L(\varphi) \geq 0$ guarantees the soft-switching of the devices s_2 and s_3. Applying these limits in (9.6) and (9.7), the ZVS boundaries conduction is obtained and described in (9.9). Accordingly, the area constrained by (9.9)

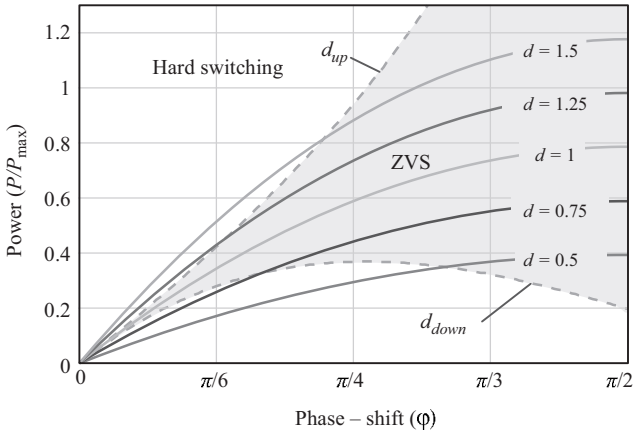

Figure 9.15 Output power of the DAB converter in function of phase-shift angle φ, considering several input–output voltage relation d

indicates the soft-switching region of the DAB converter, which is the desired operation region to reduce losses.

$$\begin{cases} d_{ZVS(up)} = 1 - \dfrac{3\varphi}{2\pi} \\ d_{ZVS(down)} = \dfrac{1}{1 - (3\varphi/2\pi)} \end{cases} \tag{9.9}$$

Figure 9.15 shows the variation of the normalized power as a function of the phase-shift angle for different values of d, in which the soft-switching boundaries are highlighted. Note that the DAB converter operates in soft-switching for the entire range of load if $d = 1$, i.e., $V_i = nV_o$. Consequently, the DAB converter can be properly designed, so that it operates with soft-switching for the whole load range.

9.7.3 Current stresses on the DAB

To calculate the current stresses on the semiconductors and transformer, the peak current on the LV side inductor ($I_{L_{a(pk)}}$) and MV side inductor ($I_{L_{b(pk)}}$) are required, and those can be calculated by (9.10) and (9.11), respectively.

$$I_{L_{PK(LV)}} = \frac{V_L - \sqrt{V_L^2 - 8L_{eq}f_s n V_L I_o}}{4L_{eq}f_s} \tag{9.10}$$

$$I_{L_{PK(MV)}} = \frac{I_{L_{a(pk)}}}{n} \tag{9.11}$$

Considering the current waveforms presented in Figure 9.16 for positive power flow, i.e., from MV to LV side, the current stresses on the semiconductors and transformer are calculated and presented in Tables 9.6–9.8. Table 9.6 shows the

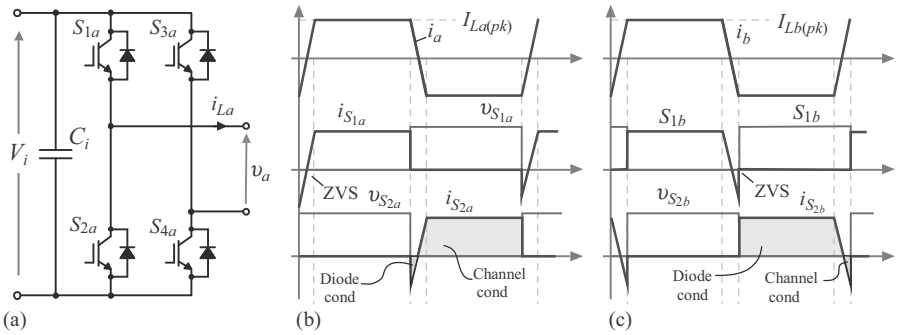

Figure 9.16 Dual active bridge: (a) topology of the active bridge and the current and voltage waveforms on the semiconductors of the (b) MV bridge and (c) LV bridge

Table 9.6 Current stresses on the semiconductor S_{1b} (MV side) of the DAB converter

Component	AVG	RMS
Channel (S_{1b})	$I_{L_{PK(LV)}}/6n(1-(3\varphi/4\pi))$	$I_{L_{PK(LV)}}/3n\sqrt{1/2(1-(5\varphi/12\pi))}$
Body diode ($i_{D_{1b}}$)	$(I_{L_{PK(LV)}}/3n)(\varphi/8\pi)$	$i_{D_{1b(rms)}} = (I_{L_{PK(LV)}}/3n)\sqrt{(\varphi/12\pi)}$

Table 9.7 Current stresses on the semiconductor S_{1a} (LV side) of the DAB converter

Component	AVG	RMS
Channel (S_{1a})	$(I_{L_{PK(LV)}}/6n)(1-(3\varphi/4\pi))$	$(I_{L_{PK(LV)}}/3n)\sqrt{1/2(1-(5\varphi/12\pi))}$
Body diode ($i_{D_{1a}}$)	$(I_{L_{PK(LV)}}/3n)(\varphi/8\pi)$	$i_{D_{1b(rms)}} = (I_{L_{PK(LV)}}/3n)\sqrt{(\varphi/12\pi)}$

Table 9.8 Current stresses on the transformer of the DAB converter

MV side i_{Lb}	MV side i_{La}
$(I_{L_{PK(LV)}}/3n)\sqrt{1-(2\varphi/3\pi)}$	$I_{L_{PK(LV)}}\sqrt{1-(2\varphi/3\pi)}$

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